thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method for forming a shunt region between two vertical N channel MOSFETs, comprising:

providing an epitaxial wafer of high resistance N– epitaxial silicon grown on top of an N+ silicon substrate and having an upper and a lower surface;

providing a mask, and then bombarding said upper surface through said mask with atomic particles having an atomic number no greater than 3.0, whereby said particles penetrate the N– silicon at least as far as said N+ layer, thereby forming an N type shunt region;

converting a portion of the shunt region, that extends a distance below the upper surface, to N– silicon; and

forming source and gate regions in said upper surface whereby an N channel shunted power MOSFET device is created.

2. The method of claim **1** wherein providing a mask further comprises depositing a layer of a metal, between about 5 and 10 microns thick, on the upper surface and then patterning and etching the metal layer.

3. The method of claim **2** wherein the metal is selected from the group consisting of tungsten and nickel/iron alloy.

4. The method of claim **1** wherein the atomic particles are protons or deuterons having an energy between about 1 and 1.6 MeV.

5. The method of claim **1** wherein providing a mask further comprises patterning and etching a metal foil to form a freestanding mask, between about 100 and 500 microns thick, that is placed between about 10 and 100 microns from the upper surface.

6. The method of claim **5** wherein the metal is selected from the group consisting of tungsten, nickel, iron, nickel/iron alloy, and aluminum.

7. The method of claim **1** wherein the step of converting a portion of the shunt region to N– silicon further comprises counter-doping by diffusing an acceptor species to a depth between about 0.5 and 5 microns.

8. The method of claim **1** wherein the step of converting a portion of the shunt region to N– silicon further comprises:

etching a trench to a depth between about 0.5 and 5 microns;

filling said trench with oxide and then polysilicon; and

removing excess oxide and polysilicon by means of chemical mechanical polishing.

9. A method for forming a shunt region within an IGBT, comprising:

providing an epitaxial wafer of high resistance N– epitaxial silicon, grown on top of a P+ silicon substrate and having an upper and a lower surface;

providing a mask, and then bombarding said upper surface through said mask with atomic particles having an atomic number less than 3.0, whereby said particles penetrate the N– silicon at least as far as said P+ layer, thereby forming an N type shunt region;

converting a portion of the shunt region, that extends a distance below the upper surface, to N– silicon; and

forming source and gate regions in said upper surface whereby an IGBT device is created.

10. The method of claim **9** wherein providing a mask further comprises depositing a layer of a metal, between about 5 and 10 microns thick, on the upper surface and then patterning and etching the metal layer.

11. The method of claim **10** wherein the metal is selected from the group consisting of tungsten, nickel, iron, nickel/iron alloy, and aluminum.

12. The method of claim **9** wherein the atomic particles are protons or deuterons having an energy between about 1 and 1.6 MeV.

13. The method of claim **9** wherein providing a mask further comprises patterning and etching a metal foil to form a freestanding mask, between about 100 and 500 microns thick, that is placed between about 10 and 100 microns from the upper surface.

14. The method of claim **13** wherein the metal is selected from the group consisting of tungsten, nickel, iron, nickel/iron alloy, and aluminum.

15. The method of claim **9** wherein the step of converting a portion of the shunt region to N– silicon further comprises counter-doping by diffusing an acceptor species to a depth between about 0.5 and 5 microns.

16. The method of claim **9** wherein the step of converting a portion of the shunt region to N– silicon further comprises:

etching a trench to a depth between about 0.5 and 5 microns;

filling said trench with oxide and then polysilicon; and

removing excess oxide and polysilicon by means of chemical mechanical polishing.

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